

REMARKS/ARGUMENTS

Summary

In this Office Action, claims 1-8 and 19-23 stand rejected. Specifically, claims 1-8 and 19-23 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 6,405,431 issued to Shin et al. (hereinafter "*Shin*"). Further, claims 19-23 stand rejected under 35 U.S.C. § 103 as being unpatentable over Shin in view U.S. Patent 6,717,264 issued to Ho et al. (hereinafter "*Ho*"). Thus, claims 1-8 and 19-23 currently are pending.

Claim Rejections under 35 U.S.C. § 102(a)

Claims 1-8 and 19-23 stand rejected under 35 U.S.C. § 102(b) as being anticipated by *Shin*. Applicants respectfully submit that amended independent claims 1 and 19, and claims 2-8, and 20-23 which depend from said independent claims, are allowable over *Shin* because at a minimum, *Shin* fails to anticipate each an every limitation of the claimed invention.

Independent claim 1, as amended, is directed to an electronic substrate comprising a substrate having two or more electrically conductive inner layers, and one or more interconnect cavities extending into, but not through, the substrate, each exposing two or more of the two or more electrically conductive inner layers. Further, the electronic substrate comprises an interconnect material disposed at least partially within one of the interconnect cavities, the interconnect material configured to electrically couple and simultaneously contact each of a surface mount technology component and the two or more of the electrically conductive inner layers.

In contrast, *Shin* cannot be said to teach one or more interconnect cavities, each exposing two or more of two or more electrically conductive inner layers. Rather, *Shin* teaches a via **69a** that is plated. See *Shin*, fig. 6c, **64**. Thus, *Shin*'s via **69a** isolates rather than exposes inner layers. Accordingly, *Shin* fails to anticipate the recited interconnect cavities. Even if *Shin*'s via could be said to expose inner layers, *Shin*

cannot be said to teach an electronic substrate comprising an interconnect material disposed in part outside one or more of the interconnect cavities and in part inside the one interconnect cavity, the interconnect material configured to electrically couple and simultaneously contact each of a surface mount technology component and the two or more of the electrically conductive inner layers. Rather, *Shin* teaches a via **69a** that is electroplated thus requiring some other form of contacting means (e.g., a solder ball) to electrically contact a surface mount technology. Further, *Shin*'s electroplated via prevents any such means from having simultaneous contact with each of a surface mount technology component and two or more electrically conductive inner layers. Therefore, for at least the reasons discussed above, Applicants respectfully submit claim 1 is patentable over *Shin*.

Claim 19, as amended, includes similar features as claim 1 and therefore is also patentable over *Shin*. Claims 2-8, and 20-23 depend from one of claims 1 and 19, and for at least the same reasons discussed above as they relate to claims 1 and 19, also are patentable over *Shin*.

Claim Rejections under 35 U.S.C. § 103

Claims 19-23 stand rejected under 35 U.S.C. § 103 as being unpatentable over *Shin* in view of *Ho*. *Ho* does not remedy the above-discussed deficiencies of *Shin* and thus, for at least the same reasons discussed above, claim 19 remains patentable over *Shin* even when combined with *Ho*. Furthermore, claims 20-23 depend from claim 19, thereby incorporating the limitations of claim 19, and therefore also are patentable over *Shin* even when combined with *Ho*.

CONCLUSION

In view of the foregoing, Applicants respectfully submits that claims 1-8, and 19-23 are in condition of allowance. Thus, entry of the offered amendments and early issuance of Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,

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